source line 4. Layers of insulating materials 5 insulate floating gate 1, substrate 2, source regions 3 and source line 4 from each other. Control gates are formed by first forming a layer 6 of conductive material (such as polysilicon) over the structure, as shown in Fig. 1A. An anisotropic poly etch is then performed to remove layer 5 except for spacer portions that form the control gates, as illustrated in Fig. 1B. The problem with this configuration is that the control gate spacers 6 have sloped side wall profiles 7 that are difficult to insulate so the remaining features of the memory cells (such as drain region and electrical contacts connected thereto) can be formed. As illustrated in Fig. 1C, insulation spacers 8 can be formed against part of the sloped sidewall portion, but most of the sloped side wall portions of control gates 6 are still exposed.